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Ultra-High Performance System Solution

Fully integrated 1G bit PHY+MAC+UOE+DMA+PCIe+Host_IF

On Select High End FPGA boards

SB 1G UOE-NIC (Ultra-Low Latency XUOE+PCIe-Board)

Top Level Product Specifications

Most Reliable, Easiest and Fastest Time to Market cycle

System board with Fully Integrated Complex Mega-IP Cores, ported and network tested, running on Xilinx/Altera FPGAs. System provides ultra-high performance NIC functionality. Intilop employs best of the breed FPGA design, simulation and implementation tools and practices to accomplish this feat.

Board incorporates second Generation UOE with 'Ultra-Low Latency' and Ultra-High Performance with highest UDP bandwidth in Full Duplex. Network Tested and mature UDP protocol offload implementation.

Board Key Features:

- **Fully Integrated and Network tested System Solution running on Select Altera/Xilinx FPGA boards, providing; SXUOE+MAC+PHY+Host_I/F SoC IP bundle.**
- **Fastest integration cycle and time to market; Just drop in your logic.**
- **Ultra-Low Latency through 1 G UOE = less than 250 ns**
- **Ultra-High Throughput: Receives and Sends sustained large UDP payloads, depending upon remote server/client's capability.**
- **Benchmark Latency and Performance results for the full system available upon request.**

Time to Market with minimal Risk:

SB 1G UOE-NIC **is the only board that integrates a Full 10G UDP Offload Engine, Ethernet MAC, PHY-Layers, Host_CPU_I/F on Select Xilinx/Altera FPGA boards so customers can easily deploy their own differentiated design on an ultra-high performance FPGA board running their application. This allows them to save months of valuable engineering time and resources in porting complex set of IPs to a FPGA platform, instead they can simply concentrate on their own design for ultra-fast system implementation and time to market with minimum risk.**

Intilop offers a wide range of Systems with Pre-integrated 1G and 1G TOE/UOE hardware cores for various end user applications. They include systems with Mutiple MAC+UOE, PCIe –Gen 2 or Gen 1 in x1/4/8 configurations, QDRx interfaces, DDRx interfaces and more. The standard System board features PCIe/DMA software driver and API that allows easy integration with customer's applications running in Linux/host environment. This can also save them months of development time allowing them to concentrate on their own software application development.

SB 1G UOE-NIC **is the only board that implements a full 1G bit PHY+MAC+UDP Full Offload Stack in Handcrafted, Ultra-Low latency and High Performance, flexible and scalable architecture which can also be easily customized for end product differentiation.**

SB 1G UOE-NIC **is flexible and customizable for layer-3, layer 4-7 network infrastructure and network security systems applications, NICs, SAN/NAS, Network Appliances and data center equipment design applications. System contains Pre integrated and tested key IP building blocks for easy customer logic integration and deployment.**

Ultimate Performance Boost for your Network Bandwidth & ROI:

SB 1G UOE-NIC **can process UDP/IP sessions as client/server in mixed session mode for Network equipment and in-line network security appliances, simultaneously, at 10-G-bit line rate. This relieves the host CPU from costly UDP/IP software related session setup/tear down, data copying and maintenance tasks thereby delivering 10x to 20x UDP/IP network performance improvement when compared with UDP/IP software.**

The 1G Bit UOE is based upon the proven and mature patent pending TOE architecture from Intilop corporation.

The same architecture is scalable to 40 G bit.

UOE System includes:

• **Generic UOE for Network infrastructure design applications:**

a) Very high performance DMA blocks also available to integrate with high performance PCIe Gen-2 x 8 interface.

b) PCIe/Driver for Linux.

• **UOE with enhanced features (available upon request)**

- All of the options available in Standard UOE plus;

i. IP and Port number filter block

ii. Specific IP and Port Filtered traffic routed to optional selected MAC interface/s or PCIe interface or Memory interface directly at line rate without CPU involvement.

iii. MAC Filter block, traffic routed to any of the selected interfaces

Benefits of Intilop UOE:

Featuring APIs at different levels the General UOE allows the application developer to easily migrate from software, to UOE hardware, to custom hardware, to achieve higher performance.

Latency:

Board Latency Comparisons	Traditional NICs running UDP Software	Intilop H/W Acceleration
Wire to User_FIFO	10 – 20 us (in NICs with TOE)	600 – 800 ns (incl PHY+MAC+TOE)
Wire to Host Memory	20 – 30 us	1.5 – 6 us (Host+driver dependent)

• 2 G throughput.

• Very low application to application latency

• Scalable solution; 40G

APIs

Network applications use the Socket API. Typically OS implements the Socket API with a UDP/IP software stack. However, the Intilop UOE implements a standard Hardware API that bypasses the Kernel, places the user_payload data directly in user_space allowing next higher level applications to fully take advantage of UOEs full hardware Offload.

Optionally, to achieve higher performance, Intilop has implemented an equivalent Socket API named UOE Socket API through PCIe driver which enables plug and play acceleration through a simple intercept of legacy standard calls.

• Hardware API: Enables dedicated processing in the FPGA for application specific acceleration

- Ideal for Very high performance specialized, differentiable ASICs or FPGAs for Financial Applications or Network infrastructure applications

- Fully verified using comprehensive verification methodology for ASIC ports and Network system tested core.

- Smallest logic foot print; less than 30,000 Xilinx slices, Altera ALMs or 250,000 ASIC gates + on-chip memory

- Fully integrated 1 G bit high performance Ethernet MAC.

- Scalable MAC Rx FIFOs and Tx FIFOs make it ideal for optimizing system performance.

- Hardware implementation of UDP stacks' control plane and data plane.

- UDP/IP unicast or Broadcast

- Hardware implementation of ARP protocol processing.

- Hardware implementation of ICMP/Ping Replies.

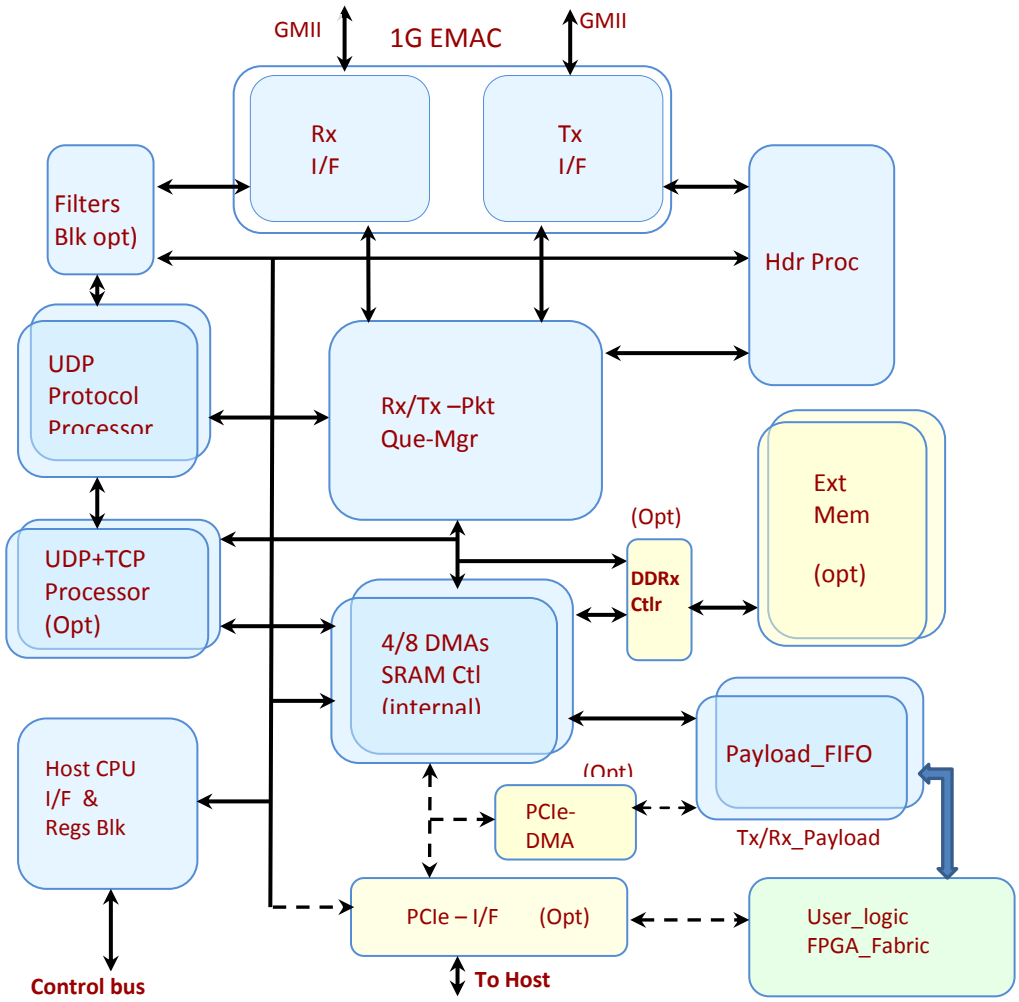
- Extended ARP table creation, deletion management (optional)

1 G Bit UDP Offload Engine (UOE) – Fully Integrated FPGA board

- Hardware implementation of ICMP or Ping processing/Replies.
- Filters for IP addresses and UDP Port numbers
- Non-UDP Bypass mode lets all Non UDP related traffic go directly to host interface via user_fifo for UDP software to handle
- Can be deployed behind a gateway which will respond to Gateway-IP request as opposed to ARP request
- On-chip DDR or SSRAM memory controller which can address from 4K Bytes to 4 MB Bytes on chip or 256 MB off chip memories (optional)
- Simple User Side interface for easy hardware integration or a little more complicated for more power full and controlled 'Streaming' data transfers.
- Many trade-offs for some functions performed in hardware or software
- Configurable Packet buffers, Port table buffers On-chip or Off-chip memories, attached DDRx interface. Depending on system, performance, ASIC/FPGA size requirements-> **User Customizable, (optional)**
- Interfaces directly to GMII, 1G Bit serial interfaces. SGMII (opt)
- Architecture can be scaled up to 40-G bits
- Integrated PLB interface (Xilinx) or Altera PLB. AXI bus interface available
- Integrated AMBA 2.0 interface or MIPs CPU bus for Local Processor control. (opt)
- User programmable/prioritize-able interrupts
- Wire-speed 20-Gbps Ethernet performance in full duplex
- UDP + IP check sum generation and check performed in hardware in less than 3 clks (20 ns at 156 MHz) vs 1-2 us by typical software UDP-stack
- User programmable Session table parameters
- Dedicated set of hardware Timers for each UDP session (opt) or customizable for sharing one set of common timers for all stale sessions.
- Direct Data placement of payload data in Applications buffer at full wire speed without CPU-> reduces CPU's buffer copy time and utilization by 95%
- Support VLAN mode (optional)
- Easily customizable for filtering various IP and UDP traffic Protocols, directed towards any port or IP (Ideal for Trading Appliances)
- Implements Full UDP Offload. No CPU involvement at any stage
- Future Proof- Flexible implementation of UDP Offload

1 G Bit UDP Offload Engine (UOE) – Fully Integrated FPGA board

- Fully integrated and FPGA ported PHY+MAC+UOE+PCIe+Host_IF System (opt)
- Basic mini API available for easy integration with Linux/windows. Others OSs/CPUs also available
- Fully integrated SoC with PHY+MAC+UOE+PCIe/DMA and driver
- Future UDP Specs updates easily adaptable



1G UDP Offload Engine + EMAC (Simplified Block Diagram)

Standard UOE UOE Options User Design

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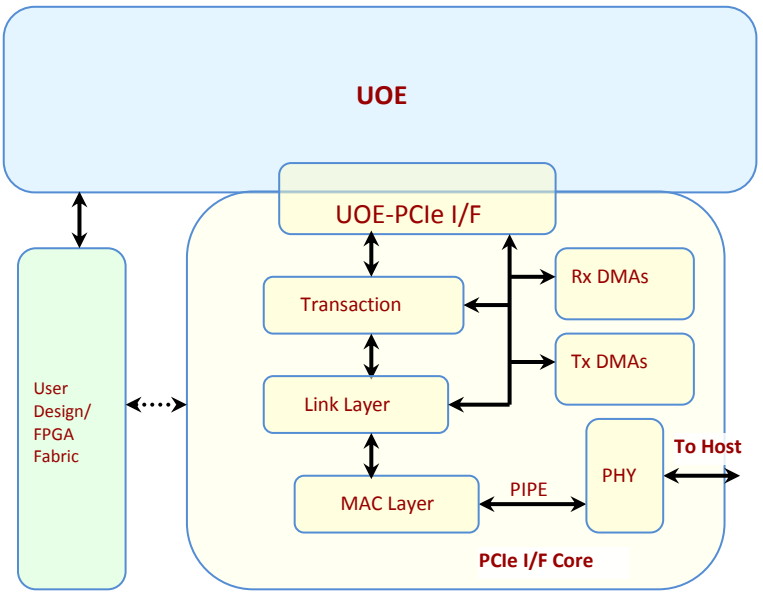
PCI Express IP core and UOE+PCIe FPGA NIC Key features:

- Compliant with the PCI Express® Base Specification, revision 2.0 and 1.1
- Supports Native and Legacy Endpoint: x1, x4, x8 lanes
  - 1 Virtual Channel (VC) with standard UOE+DMA+PCIe NIC System
  - Up to 32 PCIe Virtual Channels available as Option
- Direct UOE Register access via PCIe interface.
- Dedicated and independent high performance UDP Payload Data Path between UOE and PCIe
- UOE-PCIe driver API for easy Linux Host System Application integration
- Standard UOE+PCIe+DMA FPGA-NIC implements up to 4 DMAs.
- Includes Physical, Data Link, Transaction, and EZDMA Application layers
  - Optimized for high throughput and minimal latency
- PIPE interface to PHY
  - 16-bit/125Mhz or 8-bit/250Mhz
- Maximum payload size up to 2KB
- Number of outstanding read requests: up to 16
- Up to 6 BARs plus expansion ROM
- DMA-based user's interface
  - Up to 8 DMA channel option
  - Scatter-Gather support with host based descriptors
  - Integrated DMA arbitration optimized for maximum throughput
  - PCIe Standard Linux Driver with fully Integrated FPGA-NIC-System/development Kit
- Ultra-High Performance, Ultra-low latency PCIe driver with fully Integrated FPGA-NIC-System/development Kit, available as Option



UOE + DMA + PCIe (Simplified Diagram)

Standard UOE UOE Options User Design

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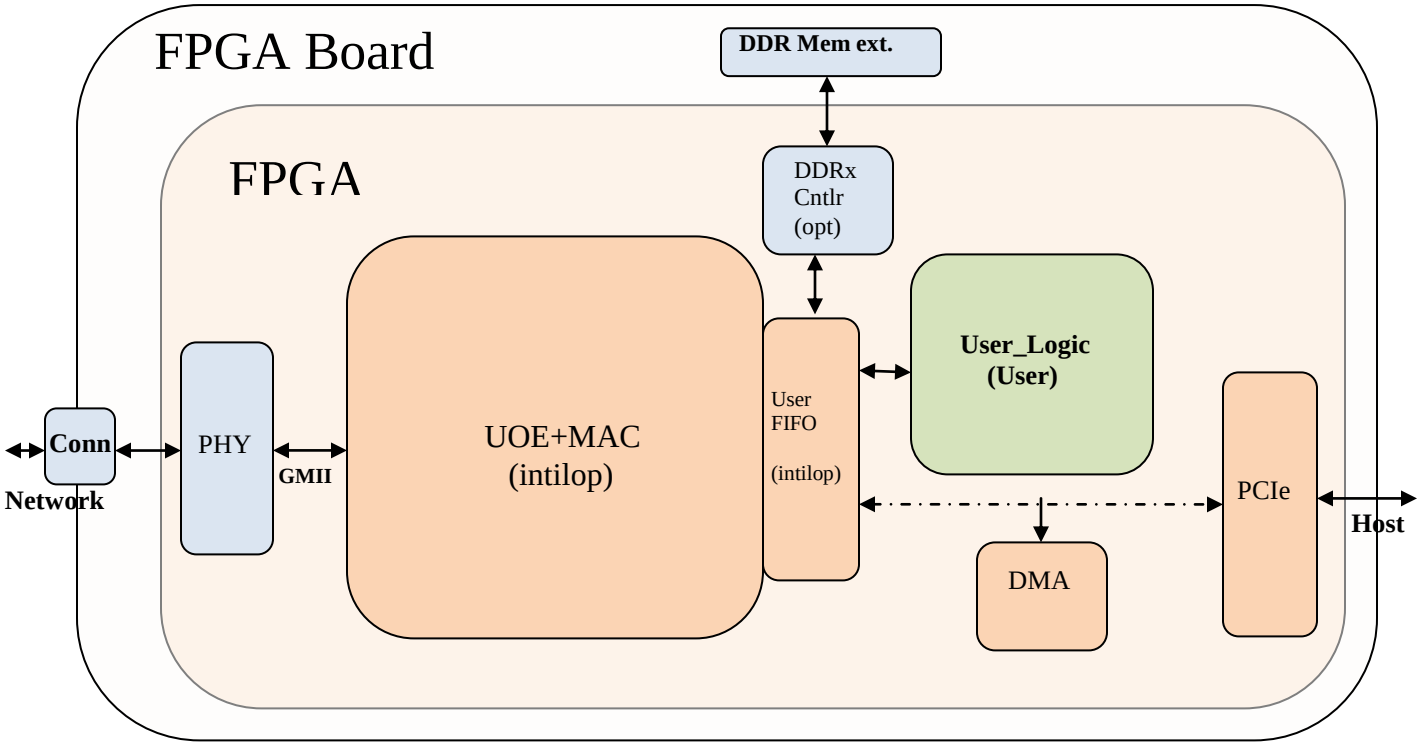

FPGA Development System with fully integrated and tested;
PHY+MAC+UOE+PCIe+DMA+Host_IF available as an option

Board and FPGA Specifications available at:

FPGA Vendors: **www.Altera.com**

www.Xilinx.com

Board Vendors: **www.bittware.com**

www.hitechglobal.com

www.Nallatech.com

www.plda.com

www.terasic.com

Deliverables:

- FPGA board/Project files.
- IP NetList.
- System Networking test software.
- Test Bench, ,vcd files, configuration code/API for easy Linux port
- Verilog models for various components e.g. UDP/IP Client and Server models, transaction model (optional)
- External memory interface/model (optional).
- UDP Model (optional)
- Verification suite (optional)
- Test packet-traffic suite (optional)

CONTACT: info@intilop.com for latest system Specifications

Full FPGA Solutions License Purchasing Options:

- **Fully Integrated/Ported IP cores and Network tested FPGA development System Platform with specified interface options**
- **IP Customization and Customer Hardware and or Application Software integration services.**

Contact sales@intilop.com for details